AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A device comprising:

a non-volatile memory storing information to load a plurality of configuration registers of a device during a memory design validation test, wherein the information includes a plurality of address information and a plurality of data corresponding to the plurality of address information, each of the plurality of address information identifying at least one of the plurality of configuration registers to which a corresponding data should be written, wherein the non-volatile memory has a maximum memory size less than a memory size sufficient to fill all the configuration registers.

2. (Original) The device of claim 1, wherein the non-volatile memory is an Electrically Erasable Programmable Read-Only Memory (EEPROM) and the configuration registers are used to define parameters for communication between the device and at least one other device.

3. (Original) The device of claim 1, wherein the plurality of configuration registers include internal configuration registers of an analog communication device.

4. (Original) The device of claim 1, wherein the device is one of a processor, a memory controller, and an Ethernet controller.

5. (Canceled)

6. (Original) The device of claim 1, further comprising a block of control logic coupled to the memory, the block of control logic to write the plurality of data to the plurality of configuration registers according to the plurality of addresses information.

7. (Original) The device of claim 1, wherein the plurality of configuration registers are to be loaded during an initialization of the device.

8. (Previously Presented) A method comprising:

resetting each of a plurality of configuration registers of a device to a register default data value; then

loading the plurality of configuration registers according to information stored in a non-volatile memory, wherein the information in a memory includes a plurality of address information and a plurality of data corresponding to the plurality of address information, each of the plurality of address information identifying at least one of the plurality of configuration registers to which a corresponding data should be written, further comprising repeating the resetting and loading to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile memory during a memory design validation stage.

9. (Original) The method of claim 8, wherein loading occurs during initialization of a communication controller device.

10. (Previously Presented) The method of claim 8, further comprising:

updating the information stored in the non-volatile memory with a second plurality of address information and a second a plurality of data corresponding to the second plurality of address information, each of the second plurality of address information identifying at least one of the plurality of registers to which a corresponding one of the second plurality of data should be written.

11. (Previously Presented) A method comprising:

a) selecting a desired configuration of a device, the desired configuration associated with desired data to be stored in a plurality of registers of the device;

b) storing test information associated with the desired configuration in a memory;

c) resetting each of the plurality of registers to a register default data value;

d) loading at least two of the plurality of registers according to the test information during a memory design validation stage, wherein the test information includes a plurality of test address information and a plurality of test data

corresponding to the plurality of test address information, each of the plurality of test address information identifying at least one of the plurality of registers to which a corresponding test data should be written;

e) identifying a subset of the plurality of test data that correspond to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration prior to loading.

12. (Original) The method of claim 11, wherein the test information includes a register address and corresponding register data for each one of the plurality of registers.

13. (Original) The method of claim 11, wherein each of the plurality of test data is a data word of register data, and each of the plurality of test address information is a data word of register test address information corresponding one of the data words of register data.

14. (Canceled)

15. (Previously Presented) The method of claim 11, further comprising identifying an additional subset of test data that corresponds to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration, after loading.

16. (Original) The method of claim 11, wherein resetting and loading occur during initialization of a communication controller device.

17. (Original) The method of claim 11, further comprising generating a desired information associated with the desired configuration, wherein generating comprises:

if there exists at least one of the plurality of test data corresponding to one of the plurality of registers having default data values equal to desired data for achieving the

desired configuration prior to loading, then storing subsequent test information and repeating c), d), and e) using the subsequent test information;

else identifying the desired information to be the test information.

18. (Original) The method of claim 17, further comprising selecting a desired memory that is less than or equal to a memory size sufficient store the desired information.

19. (Original) The method of claim 18, wherein selecting a desired memory includes reducing a size of the memory by a memory size sufficient to store the subset of the plurality of test data and the corresponding test address information.

20. (Currently Amended) A system comprising:

a plurality of configuration registers of an Ethernet controller device;

a non-volatile memory configured to store information to load at least two of the plurality of configuration registers, wherein the information in the non-volatile memory comprises a plurality of address information and a plurality of data corresponding to the plurality of address information, each of the plurality of address information identifying at least one of the plurality of configuration registers to which a corresponding data should be written; and

a block of control logic coupled to the non-volatile memory, the block of control logic adapted to write the plurality of data to the plurality of configuration registers according to the plurality of address information during a memory design validation test, wherein the non-volatile memory has a maximum memory size less than a memory size sufficient to fill all the configuration registers.

21. (Original) The system of claim 20, wherein the memory is an Electrically Erasable Programmable Read-Only Memory (EEPROM).

22. (Canceled)

23. (Canceled)

24. (Previously Presented) The method of claim 11 further comprising storing subsequent test information and repeating c), d), and e) using the subsequent test information.

25. (Previously Presented) The method of claim 11 further comprising repeating a multi-stage test data loading process, wherein repeating comprises storing subsequent test information and repeating c), d), and e) using the subsequent test information.